REMARKS

Claims 31, 32, 34, 37, 40, 41, and 43 are cancelled, above; thus, claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 are all the claims pending in the application. Claims 1, 5, 13, 17, 25, and 29-44 stand rejected on prior art grounds. Claims 5, 29-32, and 39-41 are objected to. Applicants respectfully traverse these rejections based on the following discussion.

I. The Claim Objections

The Office Action argues that as per claims 5 and 29, there is insufficient antecedent basis for displaying "said guard ring graphically" (Office Action, p. 2, item 3). Applicants submit that this objection is moot in view of the currently amended claims. Specifically, claim 5 has been amended to depend upon claim 30; and, claim 29 has been amended to depend upon claim 39, wherein both claims 30 and 39 define "displaying said logic devices and said guard ring graphically".

Furthermore, the Office Action argues that as per claims 30 and 39, there is insufficient antecedent basis for "said guard ring graphically" (Office Action, p. 2, item 3). Applicants submit that the claim element "guard ring" is defined in both claims 1 and 25, in which claims 30 and 39 depend upon, respectively. Therefore, there is sufficient antecedent basis for "said guard ring" within claims 30 and 39.

Moreover, Applicants submit that the term "said" is not utilized to modify the term "graphically" in this context; rather, "graphically" is used to describe how "said guard ring" is displayed.

The Office Action also argues that as per claims 31 and 40, there is insufficient antecedent basis for "said guard ring semantically" (Office Action, p. 2, item 3). Claims 31 and 40 have been cancelled, above; and as such, Applicants submit that the objection is moot in light of the currently amended claims.

In addition, the Office Action asserts that as per claims 32 and 41, there is insufficient antecedent basis for "displaying said logic devices and said guard ring graphically and semantically" (Office Action, p. 2, item 3). First of all, Applicants would like to note that the term "semantically" is a typographical error; and that the claimed invention provides displaying said logic devices and said guard ring graphically and *schematically*.

Such features are discussed in paragraph 0040 of Applicants' disclosure, which discusses that the invention provides representation for checking and verification of guard rings "by having a graphical, schematic, *and* symbol representation" (emphasis added). In this way, the system can "visualize the presence of the guard ring, see the guard ring in the schematic representation *and* have the guard ring contained in the symbol function" (emphasis added).

As further discussed in paragraph 0043 of Applicants' disclosure, FIG. 1 illustrates a design system structure of the present invention that integrates a parameterized cell (P-cell) design 10 and definition 13 using graphical 11 *and* schematic 12 representations. Thus, in the inventive design system, both graphical 11 *and* schematic 12 representations can be created from the design 10 and definition 13 of a parameterized cell. Graphical representations illustrate how the finished circuit will physically appear, while schematic representations illustrate functional devices and the interconnections between such devices. Such features are further discussed in

paragraph 0053 of Applicants' disclosure and illustrated in Figs. 10 and 14. In view of the foregoing, the Examiner is respectfully requested to reconsider the objections to the claims.

II. The Prior Art Rejections

Claims 1, 5, 13, 17, 25, and 29-44 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ker, et al. ("Automatic Methodology for Placing the Guard Rings into Chip Layout to Prevent Latchup in CMOS IC's," IEEE, Vol. 1, September 2001, pp. 113-116), hereinafter referred to as Ker. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a method of displaying a guard ring within an integrated circuit design having logic devices, wherein the logic devices and the guard ring are displayed symbolically and schematically in a single display. Applicants traverse the rejections because Ker fails to teach many of the features defined by the claimed invention. More specifically, Ker does not teach displaying the logic devices and guard ring symbolically and schematically. Instead, only a graphical/physical layout of "instance cells", which connect guard rings to power lines, is disclosed. In addition, Ker fails to teach symbolically displaying the type of guard ring or the efficiency of the guard ring. Instead, Ker merely discloses that guard rings can be either n-type or p-type structures. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

Applicants traverse the rejections because unlike the claimed invention, Ker fails to disclose displaying logic devices and a guard ring symbolically and schematically in a single display. Such features are defined in independent claims 1, 13, and 25 using similar language.

Citing page 114 and Figures 4(a) – 4(b) of Ker, the Office Action argues that Ker discloses displaying a *graphical/physical* layout of "instance cells", wherein the instance cells connect guard rings to power lines (Office Action, p. 4, para. 4).

First of all, Ker fails to disclose displaying logic devices and guard rings *symbolically*. Applicants submit that nothing within Ker, including the portions cited by the Office Action, teaches a display showing symbolic representations.

To the contrary, as discussed in paragraph 0021 of Applicants' disclosure, the invention displays a guard ring within an integrated circuit design by displaying logic devices and the guard ring symbolically in a single display. The symbolic display comprises a parameterized symbol. The parameterized symbol displays parameters including the type of circuit, the type of guard ring and the efficiency of the guard ring.

As further discussed in paragraph 0040 of Applicants' disclosure, the invention provides representation for checking and verification of guard rings by having a symbol representation. In this way, the system can have the guard ring contained in the symbol function. Further, the invention allows for a hierarchical representation of the symbol function. The symbol function contains the information of the circuit, the inherited parameters, and graphical representation. By having a system which auto-generates a hierarchical symbol function and integrates the guard ring symbol and all of its spacings and inherited parameters (e.g. DT ring, nwell ring, n+ ring, p+ ring) a means of checking and verification of the guard ring is provided. Thus, the invention allows a guard ring symbol to be synthesized with a circuit symbol to form a hierarchical symbol.

Moreover, as discussed in paragraph 0056 of Applicants' disclosure, FIG. 13 illustrates a hierarchical structure used for the symbol hierarchy. In FIG. 13, the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130. FIG. 14 illustrates the same hierarchy in a symbol cell view where the guard ring P-cell 142 in FIG. 14 corresponds to item 131 in FIG. 13, the hierarchical ESD P-cell 141 in FIG. 14 corresponds to item 132 in FIG. 13, and the ESD with the guard ring hierarchical design 140 in FIG. 14 corresponds to item 130 in FIG. 13. This provides verification and checking means. For example, if the symbol function shown in FIG. 14 does not contain a "ring" in the symbol function, then no guard ring exists. If the symbol is required to have a guard ring and none is present, then an error may be generated (ie, the presence of the lower symbol or lack of the higher symbol). Symbol hierarchy can then be utilized to evaluate design compliance for ESD and latchup. The higher order symbol function can also store all the essential latchup and ESD metrics for evaluation of latchup robustness, guard ring efficiency, and a means of checking and verification.

Furthermore, Ker fails to disclose displaying logic devices and guard rings *schematically*. Applicants submit that nothing within Ker, including the portions cited by the Office Action, teaches a schematic display showing logic devices and guard rings.

Conversely, as discussed in paragraph 0043 of Applicants' disclosure, FIG. 1 illustrates a design system structure of the present invention that integrates a parameterized cell (P-cell) design 10 and definition 13 using graphical 11 and schematic 12 representations. Thus, in the inventive design system, both graphical 11 and schematic 12 representations can be created from the design 10 and definition 13 of a parameterized cell. Graphical representations illustrate how

the finished circuit will physically appear, while schematic representations illustrate functional devices and the interconnections between such devices.

Accordingly, it is Applicants' position that unlike the claimed invention, Ker fails to teach displaying logic devices and a guard ring symbolically and schematically. Instead, only a graphical/physical layout of "instance cells", which connect guard rings to power lines, is disclosed. Therefore, Applicants submit that Ker fails to teach the claimed feature of "displaying said logic devices and said guard ring symbolically and schematically in a single display, wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol comprising displaying parameters" as defined by independent claims 1 and 25, and "displaying said portion of said integrated circuit design as a cell having said guard ring ... compris[ing] symbolically displaying a parameterized symbol comprising displaying parameters" as defined by independent claim 13.

In addition, Ker fails to disclose displaying a parameterized symbol comprising displaying parameters, including at least one of a type of said guard ring and an efficiency of said guard ring. Such features are defined in independent claims 1, 13, and 25 using identical language.

More specifically, as discussed in paragraph 0045 of Applicants' disclosure, the invention uses the circuit-type of indication unit 20 to classify the circuit to which the guard ring is being added. From the identification of the circuit type, the invention can automatically determine the types of guard rings which are appropriate for a given circuit which allows the guard ring to be auto-generated or manually created using graphical user interface (GUI). The

matching of the circuit type can be logically compared to the guard ring type to optimize the latchup robustness and prevent electrical injection to the substrate.

As further discussed in paragraph 0049 of Applicants' disclosure, FIG. 6 shows an exemplary graphic user interface that can be utilized with the invention. As mentioned above, the invention can automatically select the appropriate guard ring or the user can select a guard ring using the graphic user interface shown in FIG. 6. A guard ring P-cell can include a number of different guard ring structures, as well as a plurality of consecutive regions. Guard rings can be a p+diffusion ring, a n+diffusion ring, an n-well diffusion, a trench isolation (TI), a moat region, a triple well N-band region, an isolating region (forming an isolated device within the region), a deep trench (DT), a buried layer film, or an insulating film (e.g., silicon-on-insulator buried oxide region). Each type of guard ring structure is a function of the technology file and the type of structures allowed. In the technology data file, the types of possible guard rings are defined. FIG. 6 illustrates possible types of guard rings available in a specific situation. Hence, the GUI interface accesses the technology data file to define the type of guard rings available and different technologies that will require different GUI inputs.

To the contrary, Ker merely discloses that guard rings can be either n-type or p-type structures (Ker, p. 115). However, nothing within Ker teaches symbolically displaying whether the guard ring is an n-type or p-type structure. Moreover, nothing within Ker teaches symbolically displaying any of the parameters of the guard rings.

Furthermore, in regards to guard ring efficiency, paragraph 0052 of Applicants' disclosure discusses that the relative placement (spacing) of the two P-cells (the input node ESD P-cell and the guard ring P-cell) will allow evaluation of the parasitic elements formed between

the first and second P-cells. For example, a lateral npn can be formed between the ESD P-cell well, and the guard ring (if of n-type dopant). This parasitic npn can be represented as an additional circuit element within the hierarchical P-cell and can be used to evaluate the injection to the guard ring P-cell and its effectiveness in absorbing electrical current. In this fashion, *the guard ring efficiency can be evaluated based on its effectiveness in collecting and absorbing electrical transient currents*, noise injection, and other latchup inducing sources of current. This information can be stored in the higher hierarchical P-cell information for evaluation of latchup sensitivity from internal or external sources. Hence, the integration of the first and second parameterized cells (the input node ESD P-cell and the guard ring P-cell) leads to the ability to evaluate latchup, guard ring efficiency, and the interaction between the first ESD P-cell and its adjacent guard ring. In this fashion, circuit simulation can be performed and latchup sensitivity can be evaluated as a result of the P-cell circuit schematic cell view that contains the parasitic information.

Conversely, Ker does not discuss the efficiency of the guard rings. There is no mention of the guard rings' ability to collect carriers. Instead, the focus of the disclosure in Ker is on the design tools' ability to reduce the series resistance of the guard ring structure. Nothing within Ker teaches symbolically displaying the efficiency of the guard ring. Moreover, nothing within Ker teaches symbolically displaying any of the parameters of the guard rings.

Therefore, in view of the foregoing, it is Applicants' position that Ker fails to disclose the claimed feature of "displaying a parameterized symbol comprising displaying parameters, including at least one of a type of said guard ring and an efficiency of said guard ring" as defined by independent claims 1, 13, and 25.

Furthermore, Applicants traverse the rejections because Ker fails to disclose displaying a guard ring within a hierarchical integrated circuit design, wherein the hierarchical integrated circuit design has a parameterized cell and at least one guard ring. Such features are defined in independent claim 13 using similar language.

More specifically, as discussed in paragraph 0048 of Applicants' disclosure, FIG. 5 is a flowchart that illustrates that the invention first identifies the type of circuit (and the type of ESD protection) 50. This allows the invention to create a parameterized cell (P-cell) 51. The invention then selects the appropriate type of guard ring and places the guard ring within the P-cell 52. *The combined guard ring and P-cell are produced and can be used in a hierarchical circuit design 53.* As further discussed in paragraph 0056 of Applicants' disclosure, FIG. 13 illustrates a hierarchical structure used for the graphical, circuit schematic, or symbol hierarchy. In FIG. 13, *the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130.*

To the contrary, nothing within Ker discloses a hierarchical integrated circuit design. Instead, Ker merely discloses an integrated circuit design having guard rings. Although the Office Action argues that Ker teaches the use of double guard rings (Office Action, p. 3, item 6), nothing within Ker discloses a hierarchical integrated circuit design including such guard rings and a parameterized cell.

Therefore, it is Applicants' position that Ker fails to teach or suggest the claimed feature of "displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring" as defined by independent claim 13.

Therefore, it is Applicants' position that Ker does not teach or suggest many features defined by independent claims 1, 13, and 25 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 5, 17, 29-30, 33, 35-36, 38-39, 42, and 44 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to

discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 10/5/06

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